DS3112RD
DS3/E3 Multiplexer Reference Design

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GENERAL DESCRIPTION

The DS3112RD is a reference design for the DS3112 DS3/E3 framer/mux and the DS3150 DS3/E3 LIU. Both devices are surface mounted to minimize board size and to provide signal integrity. The DK101/DK2000 motherboard and included software give point-and-click access to configuration and status registers from a Windows®-based PC. LEDs on the board indicate loss-of-signal, transmit driver monitor, and PRBS sync status of the LIU. The board provides BNC connectors for an external clock, the line-side transmit and receive differential pairs, and a connector for data path interface. A PLD provides registered access to the LIU control pins along with control of clock and data paths.

Each DS3112RD is shipped with a free DK101 motherboard. For complex applications, the DK2000 high-performance demo kit motherboard can be purchased separately.

Windows is a registered trademark of Microsoft Corp.

REFERENCE DESIGN CONTENTS

DS3112RD Daughter Card
DK101 Demo Kit Motherboard
CD-ROM
- ChipView Software
- DS3112RD.DEF Definition File
- DS3112.DEF Definition File
- DS3112RD Data Sheet
- DS3112 Data Sheet
- DS3150 Data Sheet

ORDERING INFORMATION

PART	DESCRIPTION
DS3112RD	DS3112 Reference Design

FEATURES

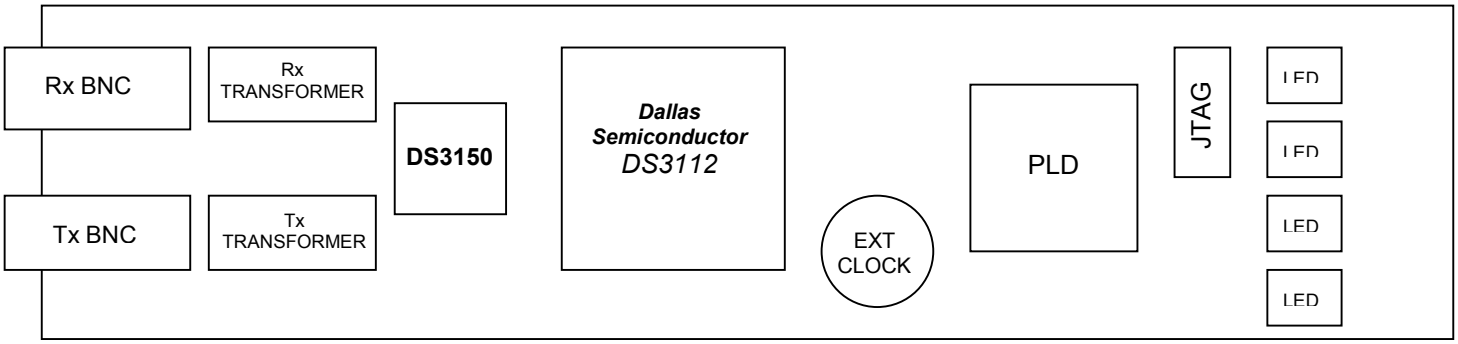
- Soldered DS3150 and DS3112
- BNC Connectors, Transformers, and Termination Passives for the LIU
- Careful Layout for Analog Signal Paths
- Memory-Mapped PLD for Control of DS3150
- BNC Connectors for External Clock and Line-Side Interface
- Compatible with DK101 and DK2000 Demo Kit Motherboards
- DK101/DK2000 and Included Software Provide Point-and-Click Access to the DS3112 Register Set
- LEDs for Loss-of-Signal, Transmit Driver Monitor, and PRBS Sync

REV: 082103

COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1–C16, C20–C27	24	0.1μF 10%, 25V ceramic capacitors (1206)	Panasonic	ECJ-3VB1E104K
C17–C19	3	0.047μF 10%, 50V ceramic capacitors (1206)	Panasonic	ECU-V1H473KBW
C28–C30	3	10μF 20%, 16V tantalum capacitors (B case)	Panasonic	ECS-T1CX106R
DS1–DS4	4	LED, red, SMD	Panasonic	LN1251C
J1, J2	2	5-pin, right-angle, BNC connectors	Trompeter	UCBJR220
J3	1	5-pin, vertical, BNC connector	Cambridge	CP-BNCPC-004
J4–J6	3	50-pin jumper, dual row	Samtec	TFM-125-02-S-D-LC
J7	1	10-pin, dual row, vertical connector	Digi-Key	S2012-05-ND
R1–R4, R8, R14, R500	7	10kΩ 1%, 1/8W resistors (1206)	Panasonic	ERJ-8ENF1002V
R5, R10	2	0Ω 5%, 1/8W resistors (1206)	Panasonic	ERJ-8GEYJ0R00V
R6, R7, R9, R11–R13	6	330Ω 0.1%, 1/10W MF resistors (0805)	Panasonic	ERA-6YEB331V
R501	1	75Ω 5%, 1/8W resistor (1206)	Panasonic	ERJ-8GEYJ750V
T1, T2	2	XFMR, 1-to-2 count, 6-pin SMT	Pulse Engineering	PE-65968
TP1–TP17	17	Testpoint, 1 plated thru-hole	—	—
U1	1	T3/E3 mux/framer	Dallas Semiconductor	DS3112
U2	1	T3/E3/STS-1 line interface	Dallas Semiconductor	DS3150T
U3	1	IC, hex interverter, SO	Toshiba	TC74HC04AFN
U4	1	IC, PLD, 100-pin TQFP	Altera	EPM7128AETC100-10
U5	1	IC, MUX, quad 2INPUT	Philips	74LVC157APW DH

BOARD FLOORPLAN



PLD MEMORY MAP

The PLD on the DS3112RD is used to route clocks from the processor board DK2000/DK101 and to control the DS3150 and the DS3112. The PLD is mapped at address 00h and contains 25 registers. The first eight registers (excluding register address 01h, which has no function on the 3112RD) are read-only, and are programmed at the factory to document board identification and revision information. The next 16 registers control the state of pins on the DS3150 and DS3112. The last register controls the clock source to the FTCLK pin on the DS3112 and the MCLK pin on the DS3150. The PLD provides tri-state control of the pins. If a 01h is written to a register, the corresponding pin is forced high, a value of 00h forces the pin low, and writing any other value puts the pin in a tri-state mode. The bit descriptions in the definition file for the DS3112RD describe how to control a pin specifically (Table 1). For more information about definition files, refer to the DK101 data sheet or the DK2000 data sheet.

MEMORY MAP

The DS3112 is mapped at 1000h.

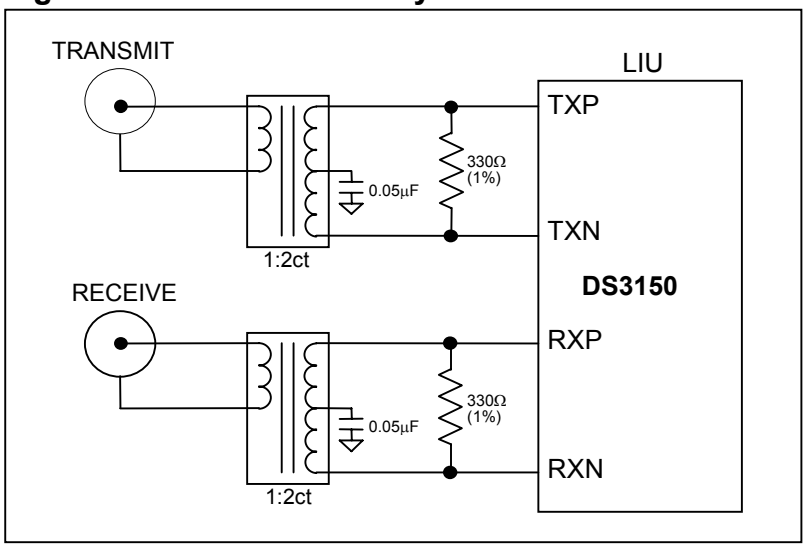
Table 1. DS3112RD CPLD Register Map

OFFSET	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
0X0000	BID	Read-Only	0x0D	Board ID
0X0002	XBIDH	Read-Only	0x00	High Nibble Extended Board ID
0X0003	XBIDM	Read-Only	0x00	Middle Nibble Extended Board ID
0X0004	XBIDL	Read-Only	0x01	Low Nibble Extended Board ID
0X0005	BREV	Read-Only	—	Board FAB Revision
0X0006	AREV	Read-Only	—	Board Assembly Revision
0X0007	PREV	Read-Only	—	PLD Revision
0X0011	TDS0	Read-Write	0x00	DS3150 Transmit Data Select 0
0X0012	TDS1	Read-Write	0x00	DS3150 Transmit Data Select 1
0X0013	EFE	Read-Write	0x01	DS3150 Enhanced Feature Enable
0X0014	ICE	Read-Write	0x00	DS3150 Invert Clock Enable
0X0015	LBKS	Read-Write	0x01	DS3150 Loopback Select
0X0016	RMON	Read-Write	0x00	DS3150 Receive Monitor Mode
0X0017	TESS	Read-Write	0x01	DS3150 T3/E3/STS-1 Select
0X0018	TTS	Read-Write	0x01	DS3150 Transmit Tri-State
0X0019	ZCSE	Read-Write	0x00	DS3150 Zero Code Suppression
0X001A	LBO	Read-Write	0x00	DS3150 Line Build-Out
0X001B	RST	Read-Write	0x01	DS3112 Reset
0X001C	MUXSEL	Read-Write	0x01	DS3112RD Data Path Mux
0X001D	G747E	Read-Write	0x00	DS3112 G747 Mode Enable
0X001E	T3E3MS	Read-Write	0x00	DS3112 T3/E3 Mode Select
0X001F	FRMECU	Read-Write	0x00	DS3112 Error Counter Strobe
0X0020	FTMEI	Read-Write	0x00	DS3112 Error Insert Strobe
0X0021	T3E3CLK	Read-Write	0x01	DS3112RD Clock Select

LINE-SIDE CONNECTIONS

The DS3112RD implements the transmit (Tx) and receive (Rx) line interface networks recommended in the DS3150 data sheet (Figure 1). The BNC connectors are labeled J1 (Tx) and J2 (Rx).

Figure 1. Line-Side Circuitry



INTERFACE CONNECTOR

Two 50-pin connectors (J4, J5) on the bottom of the board provide the processor interface, clocks, and power supply from the DK101 or DK2000 motherboards. These connectors also provide a bidirectional clock/data/sync connection with the DK2000. The third connector (J6) is provided for future expansion on the DK2000 and is not connected on the DS3112RD.

CONNECTING TO A COMPUTER

Refer to the DK101 data sheet or the DK2000 data sheet for information.

BASIC OPERATION

The DS3112RD powers up in the T3 mode, transmitting all ones, as specified by the default values in the CPLD registers (Table 1) and the DS3112's reset condition. The processor interface supplies the transmit clock by default. The user must access registers in the DS3112 and the CPLD to configure the board. To facilitate configuration, definition files that support the DS3112 reference design (DS3112.DEF, DS3112RD.DEF) can be downloaded from our website, www.maxim-ic.com/DS3112RD.

DS3112RD INFORMATION

For more information about the DS3112RD—including the ChipView software, the latest support files (.DEF, .INI, etc.), and the latest data sheet—please visit our website at www.maxim-ic.com/DS3112RD.

DS3112 INFORMATION

For more information about the DS3112, please consult the DS3112 data sheet, available on our website at www.maxim-ic.com/DS3112.

DS3150 INFORMATION

For more information about the DS3150, please consult the DS3150 data sheet, available on our website at www.maxim-ic.com/DS3150.

DK101/DK2000 INFORMATION

For more information about the DK101 or DK2000, please consult their respective data sheets, available on our website at www.maxim-ic.com/DK101 and www.maxim-ic.com/DK2000.

TECHNICAL SUPPORT

For additional technical support, please e-mail your questions to telecom.support@dalsemi.com.

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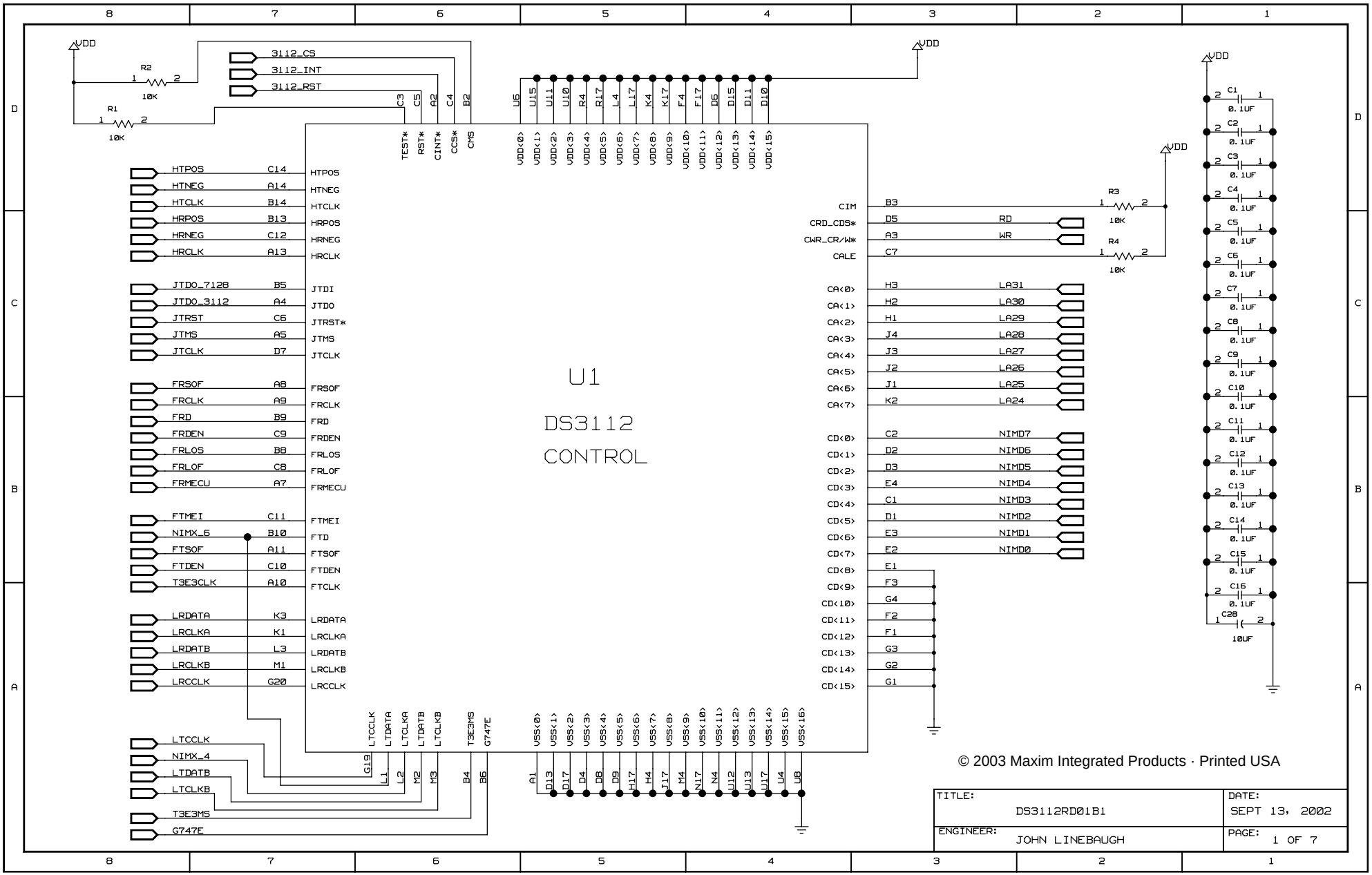

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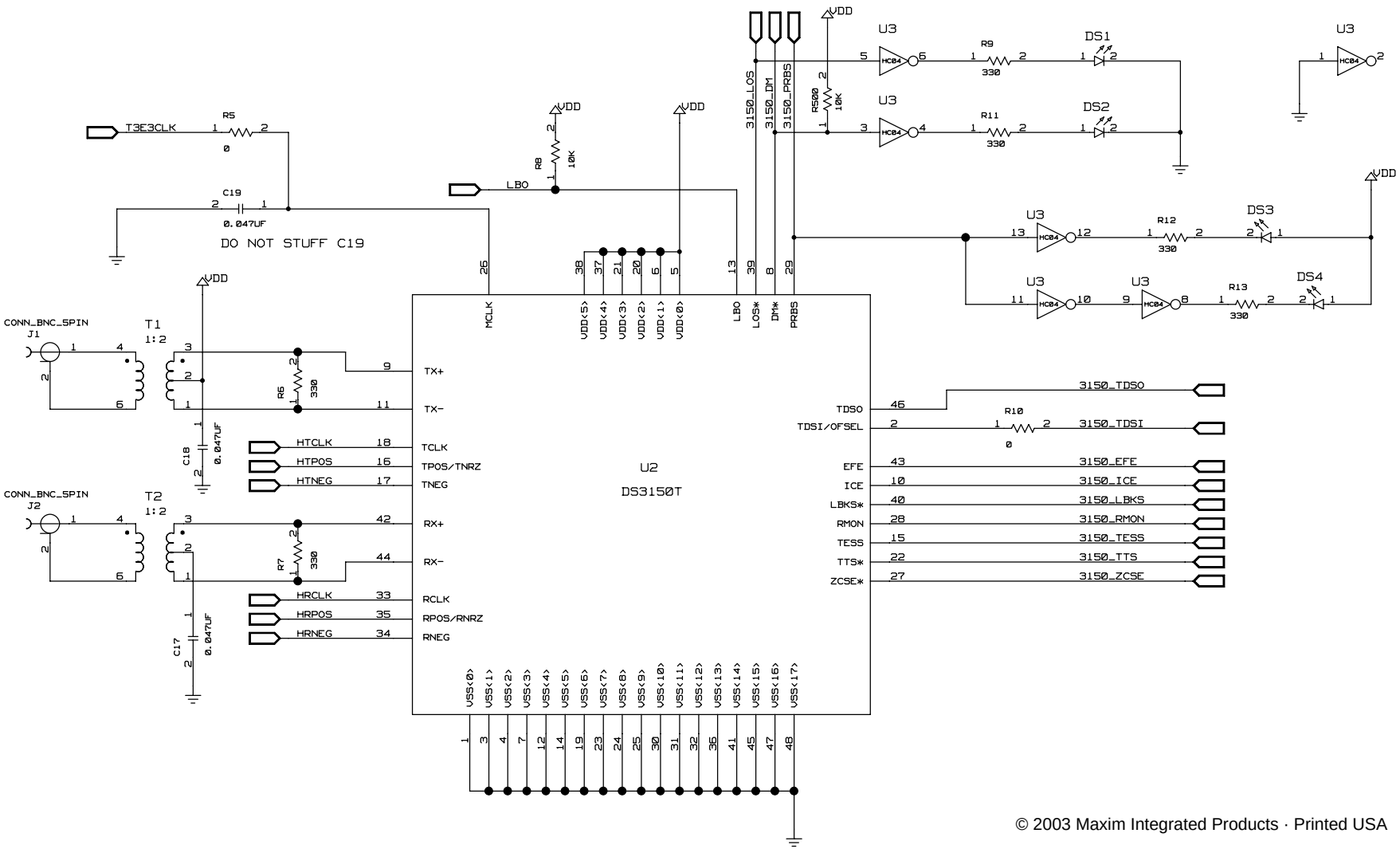
U2
DS3150T
T3E3CLK
R5
0
C19
0.047UF
DO NOT STUFF C19
LBO
R8
10K
VDD
3150_LOS
3150_DM
3150_PRBS
R500
10K
U3
HC04
R9
330
DS1
R11
330
DS2
R12
330
DS3
R13
330
DS4
CONN_BNC_5PIN
J1
J2
T1
1:2
T2
1:2
R6
330
R7
330
C18
0.047UF
C17
0.047UF
HTCLK
HTPOS
HTNEG
HRCLK
HRPOS
HRNEG
MCLK
VDD<5>
VDD<4>
VDD<3>
VDD<2>
VDD<1>
VDD<0>
LBO
LOS*
DM*
PRBS
TX+
TX-
TCLK
TPOS/TNRZ
TNEG
RX+
RX-
RCLK
RPOS/RNRZ
RNEG
TDSO
TDSI/OFSEL
EFE
ICE
LBKS*
RMON
TESS
TTS*
ZCSE*
R10
0
3150_TDSO
3150_TDSI
3150_EFE
3150_ICE
3150_LBKS
3150_RMON
3150_TESS
3150_TTS
3150_ZCSE
VSS<0>
VSS<1>
VSS<2>
VSS<3>
VSS<4>
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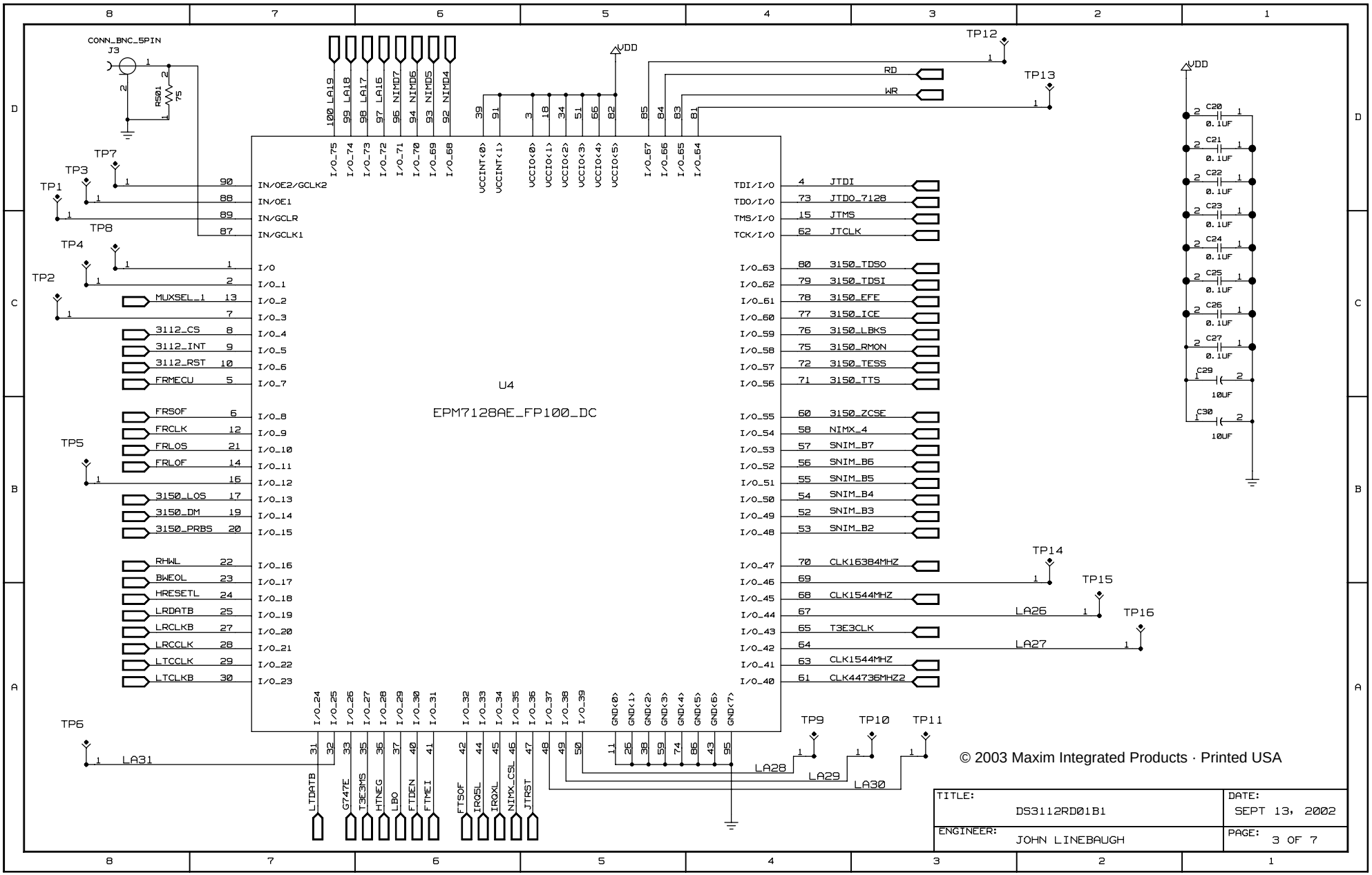

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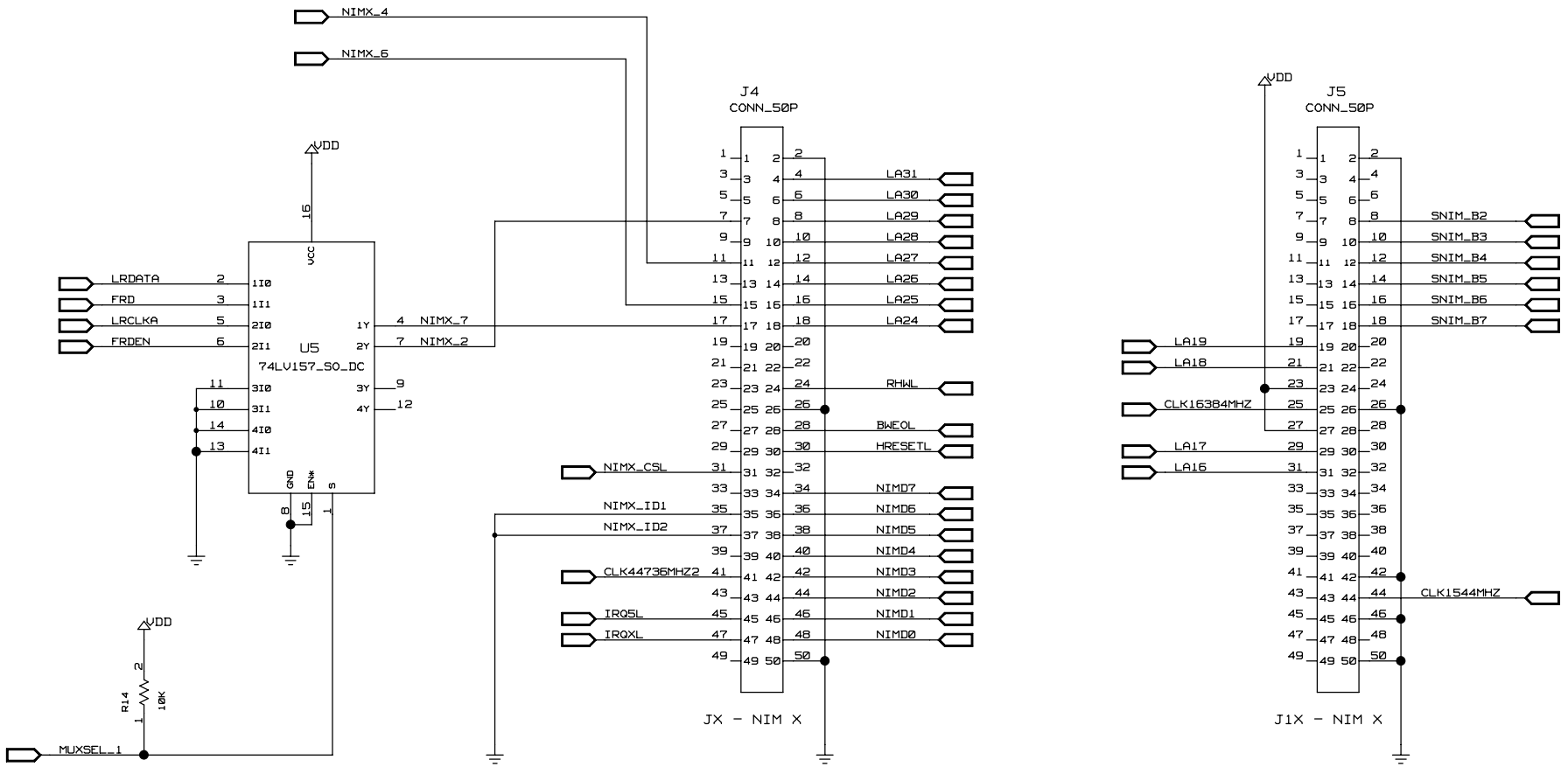

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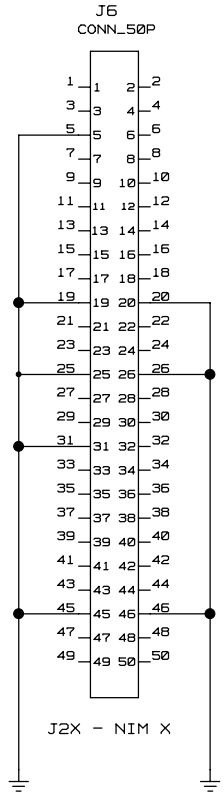

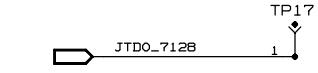

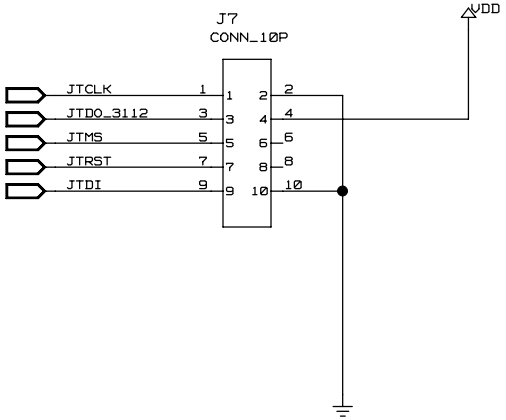

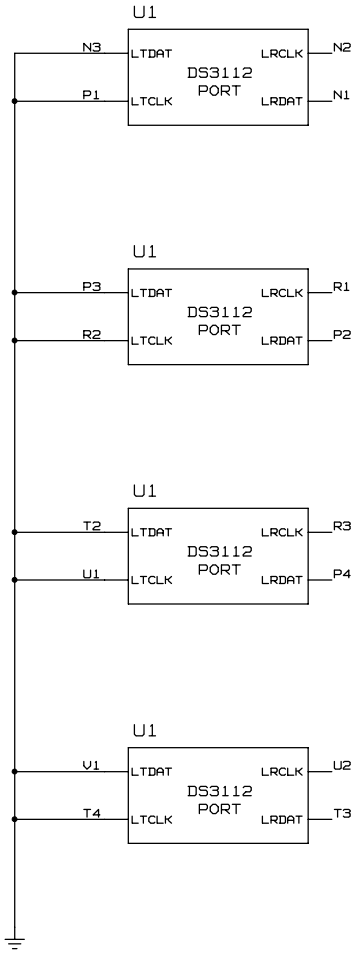

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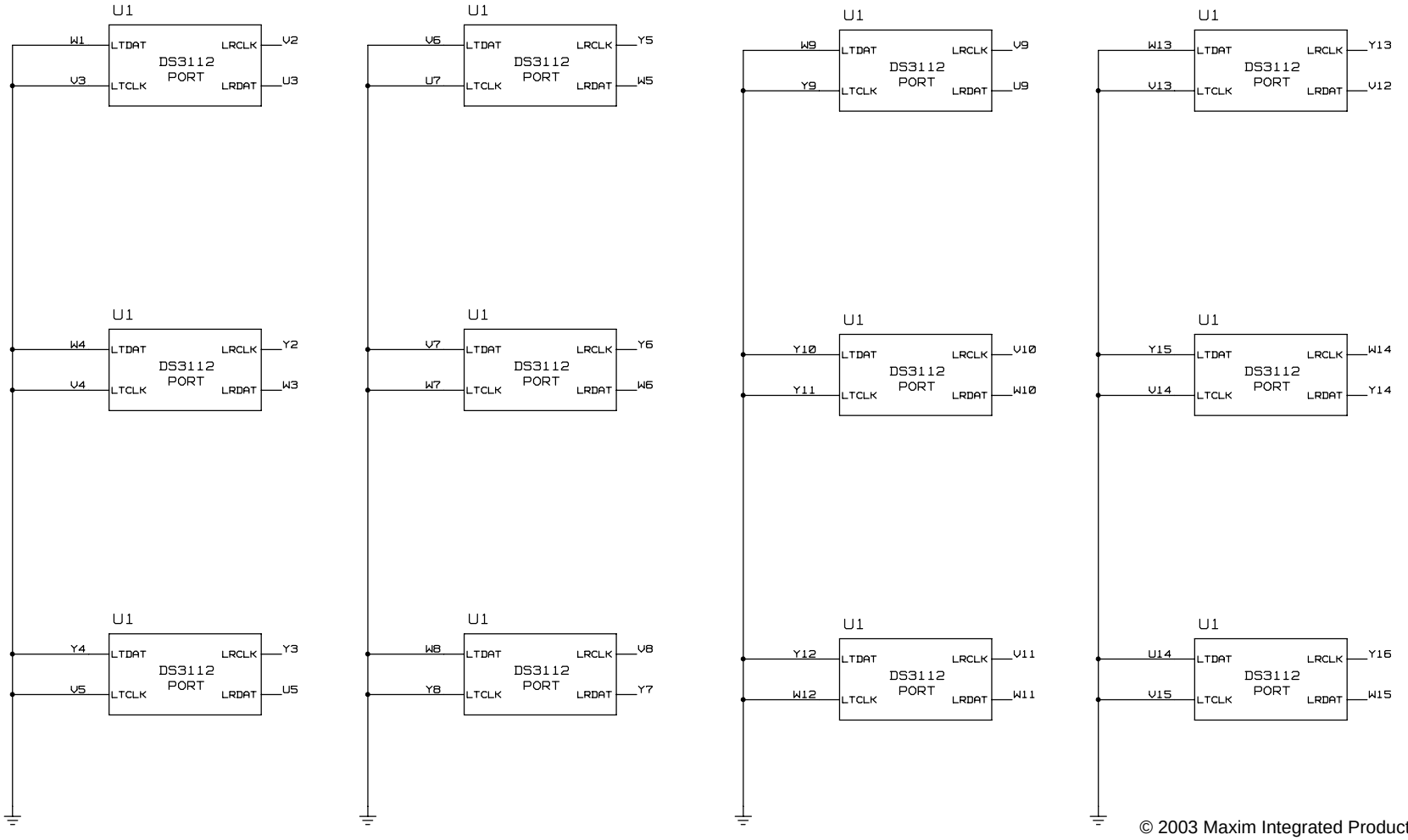

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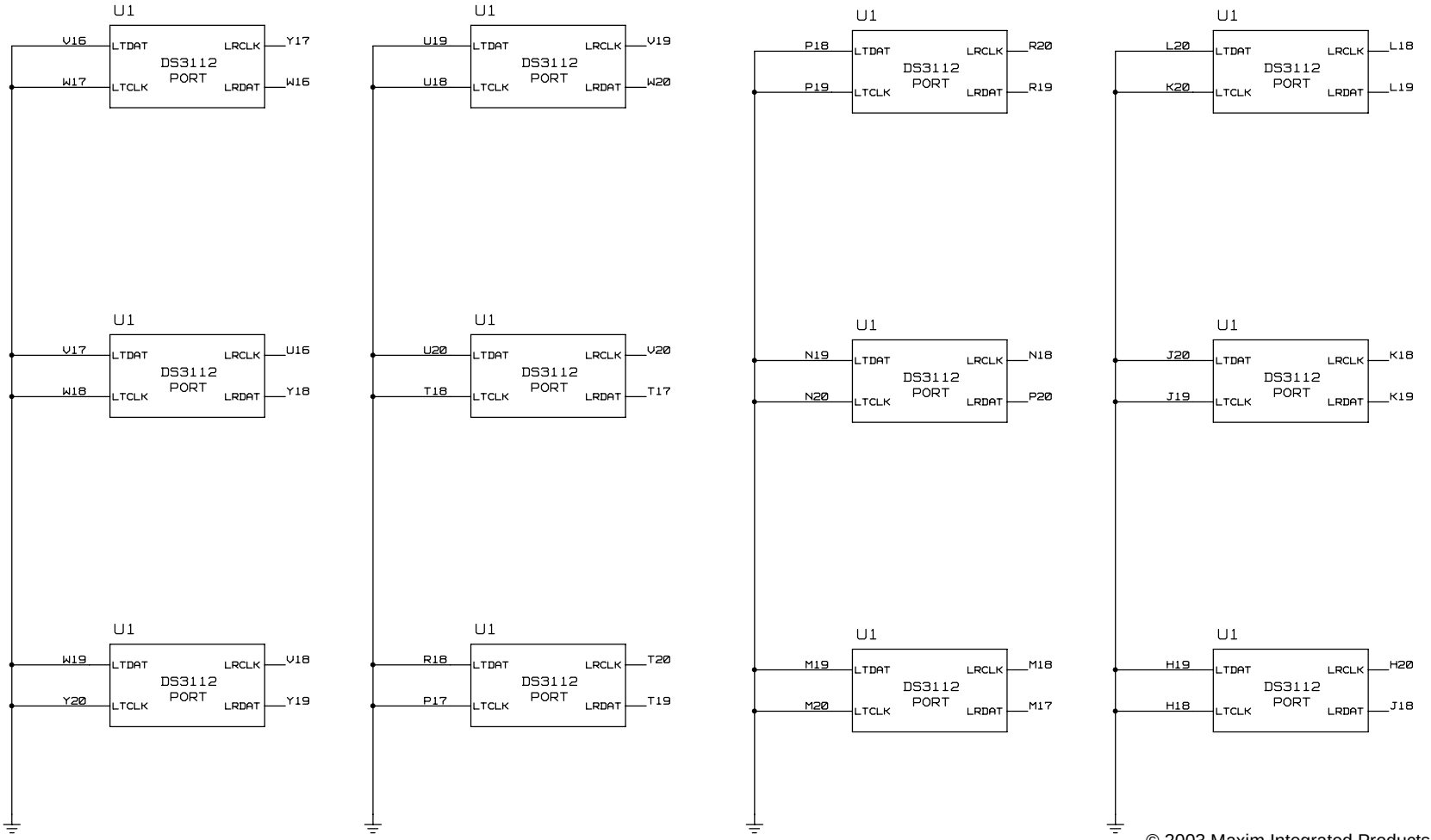

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